

# Effect of PVD process parameters on the quality and reliability of thin (10–30 nm) $\text{Al}_2\text{O}_3$ dielectrics

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Received: 4 July 2011 / Accepted: 12 September 2011 / Published online: 29 September 2011  
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**Abstract** Over the last decade, dielectric scaling in non-volatile memories (NVM) and CMOS logic applications has reached a point where better innovations will be required to meet the reliability and performance requirements of future products. For both these applications, high  $k$  materials are being explored as possible candidates to replace the traditional  $\text{SiO}_2$  and oxide/nitride/oxide-based films used today. While there are several attractive candidates to replace these materials,  $\text{HfO}_2$  and  $\text{Al}_2\text{O}_3$  are considered as the most promising ones. Although there has been a lot of work on CVD-based  $\text{Al}_2\text{O}_3$ , there has not been much reported for PVD-based  $\text{Al}_2\text{O}_3$  for NVM applications, especially in the thickness regime of 10–30 nm. This paper discusses the effects of process parameters such as plasma power and annealing conditions on the quality of  $\text{Al}_2\text{O}_3$  dielectrics. It was observed that a post deposition anneal in  $\text{O}_2$  ambient at  $700^\circ\text{C}$  for 15 s is essential to obtain a fully oxidized film with high density. While higher power (1,500 W) results in thicker films with better  $k$  values, they also lead to more substrate damage and poorer reliability. Annealing done at temperatures greater than  $700^\circ\text{C}$  for 60 s or more results in failure of the film possibly due to diffusion of silicon into  $\text{Al}_2\text{O}_3$  and its subsequent reaction.

**Keywords** High  $k$  · Non-volatile memories · PVD

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## Introduction

Aluminum oxide ( $\text{Al}_2\text{O}_3$ ) has been an interesting material having a moderate dielectric constant ( $k \sim 9$ ) and a low leakage current density (Dimoulas et al. 2007). It has been studied extensively over the past decade or so for memory and gate stack applications (Schlom et al. 2008; Lee et al. 2006). However, certain issues like fixed charges, mobility degradation, insufficient interface quality and a relatively lower  $k$  value (compared to other insulators like  $\text{HfO}_2$ ) has restricted its applicability in production (Wilk 2001; Guha et al. 2002). Hence, a great deal of the study available on  $\text{Al}_2\text{O}_3$  is for ultra-thin films ( $<4$  nm), and mostly in combination with other dielectrics as stacks (Bouazra et al. 2008; Ko 2007; Son et al. 2007). Recently,  $\text{Al}_2\text{O}_3$  has also been perceived as an attractive option for the blocking (or control) dielectric in Flash memories, owing to its high band gap (8.9 eV) which confers excellent leakage properties (Singh et al. 2008).

The role of the blocking dielectric in flash memory is to prevent the injected charge in the floating gate from leaking. In a practical scenario however, charge conduction does take place at the large fields used in the flash memory devices. The use of  $\text{Al}_2\text{O}_3$  as the blocking dielectric not only reduces the charge leakage but also, owing to its relatively higher  $k$ , increases the coupling of the storage node with the control gate thus improving the programming and erasing speeds and/or reducing the operating voltages. And as such, the ideal requirements for a blocking dielectric material would be: (a) large bandgap (b) high dielectric constant (c) good chemical and thermal stability (d) large breakdown field.

Numerous techniques have been developed over the years for depositing thin films of  $\text{Al}_2\text{O}_3$  (Kohara et al. 2004; Groner et al. 2002). However, the widely used metal

organic chemical vapour deposition (MOCVD), process for dielectric deposition has the inherent issue of organic contamination which can adversely affect the device performance (Crowell et al. 2003). Consequently, recent efforts have been aimed at refurbishing the physical vapour deposition (PVD) process to deposit thin dielectrics for flash memory devices. However, there are issues such as film conformality and stoichiometry associated with the PVD process, which are often addressed by annealing the film. Nevertheless, it demands a comprehensive study on the effects of the process parameters on the film's material and electrical properties.

This work addresses some of the lacunae in the existing knowledge and contributes to an increased understanding of the impact of certain PVD deposition parameters on the dielectric characteristics of  $\text{Al}_2\text{O}_3$  which have largely being ignored in the prior work.

### Experimental: device fabrication and electrical measurements

The metal–insulator–silicon (MIS) capacitors were fabricated using the following procedure. First, p-type Si (100) substrates having a resistivity of 0.01–0.02  $\Omega\text{cm}$  were degreased and acid cleaned using an RCA etch and an HF dip. PVD of  $\text{Al}_2\text{O}_3$  was carried out in Applied Materials' Endura using  $\text{O}_2$  flow rate of 25 sccm. The target power was varied between 500 W and 1,500 W, and substrate heating was not used. Thickness and refractive index of the films was measured by ellipsometry. Subsequent post deposition anneal (PDA) in an RTP chamber and Aluminum gate metallization (shadow mask area:  $7.85 \times 10^{-3} \text{ cm}^2$ , thickness  $\sim 150 \text{ nm}$ ) were done to complete the device fabrication process.

The electrical characterization was performed using Agilent 4155C semiconductor parameter analyzer, Keithley 4200 semiconductor characterization system, Agilent 4284 LCR meter. These instruments were connected to the low noise probe station by Keithley 708A switch matrix with low current 7174 card. The C–V measurements were carried out at 100 kHz, with the applied AC voltage peak-to-peak signal level of 50 mV. Hysteresis was extracted at  $V_{\text{fb}}$ . Flatband voltage and  $D_{\text{it}}$  were obtained using CVC Hauser program.

### Results and discussions

#### Effect of plasma power

Figure 1a shows the thickness and refractive index of unannealed and annealed samples as a function of plasma

power. Post PVD annealing was done at 700°C in  $\text{O}_2$  for 15 s to ensure complete oxidation of the films.

The films exhibit an RI value close to what is learned in literature for  $\text{Al}_2\text{O}_3$  thin films (Patil et al. 1996). Variation in refractive index is quite minimal with the change in power, and film thickness increases linearly with increasing power. For the annealed film, the reduction in thickness ( $\sim 15\%$ ) is believed to be caused by the film densification which also improves the film's refractive index.

The electrical responses of the films have been presented in Fig. 2a and b. On examining the C–V plot in Fig. 2a, it can be seen that there is a substantial shift in the C–V curves as power increases. This is due to the increased deposition power causing significant damage to the substrate which, in turn, increases the fixed charges and causes the observed shift in the flatband voltage (Fig. 3a).

Oxide charges can be calculated using the following equation:

$$V_{\text{fb}} = \phi_{\text{ms}} - \frac{Q_{\text{ox}}}{C_{\text{ox}}} \quad (1)$$

By plugging in the appropriate values,  $Q_{\text{ox}}$  for deposition powers of 500, 1,000 and 1,500 W are  $3.2\text{e}-7$ ,  $3.8\text{e}-7$ , and  $4.1\text{e}-7/\text{cm}^2$ . Higher values of oxide charges at greater power strengthen the argument that substrate damage has a direct relationship with deposition power.

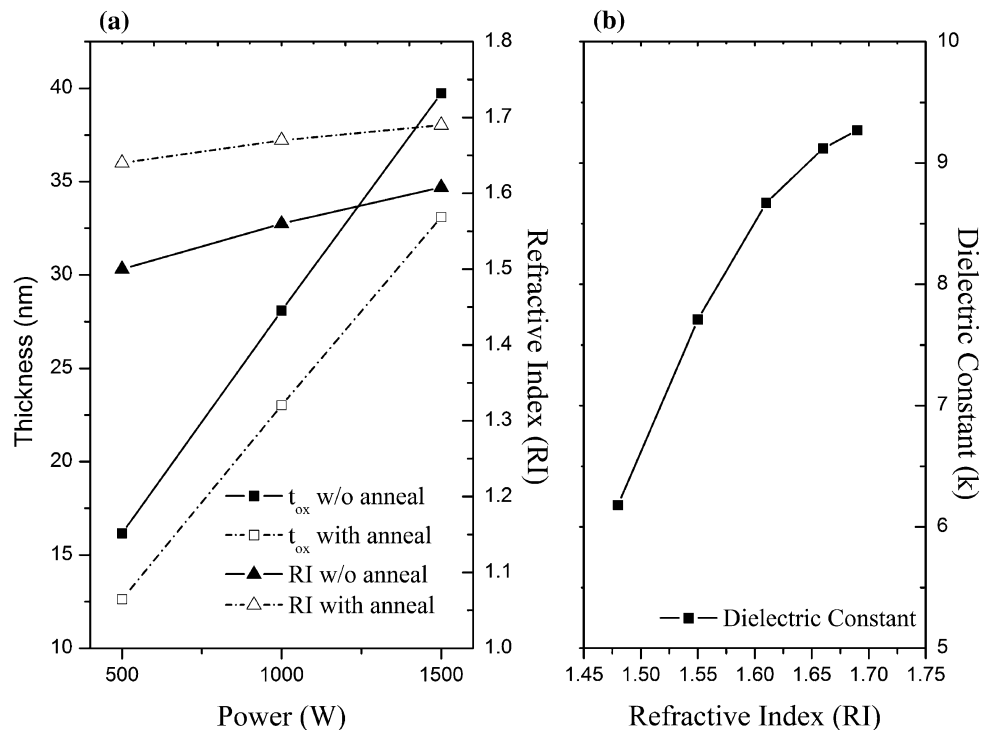
It can be seen in Fig. 3b that the hysteresis, which is a measure of (i) charge trapping in the dielectric and at the interface (ii) mobile charge carriers in the dielectric, is almost zero for plasma power of 500 W, but surges to  $\sim 90 \text{ mV}$  for 1,000 and 1,500 W. This indicates that 500 W deposition results in significantly lower damage to the substrate than depositions at 1,000 and 1,500 W. Again, from Fig. 3c, it can be observed that the depositions done at 500 W show marginally higher breakdown fields (50% failure) than the depositions done at 1,000 and 1,500 W, confirming damage to the substrate caused by higher power deposition. Typical reported values for  $\text{Al}_2\text{O}_3$  breakdown field are 6–8 MV/cm (Groner et al. 2002).

#### Effect of long duration anneals

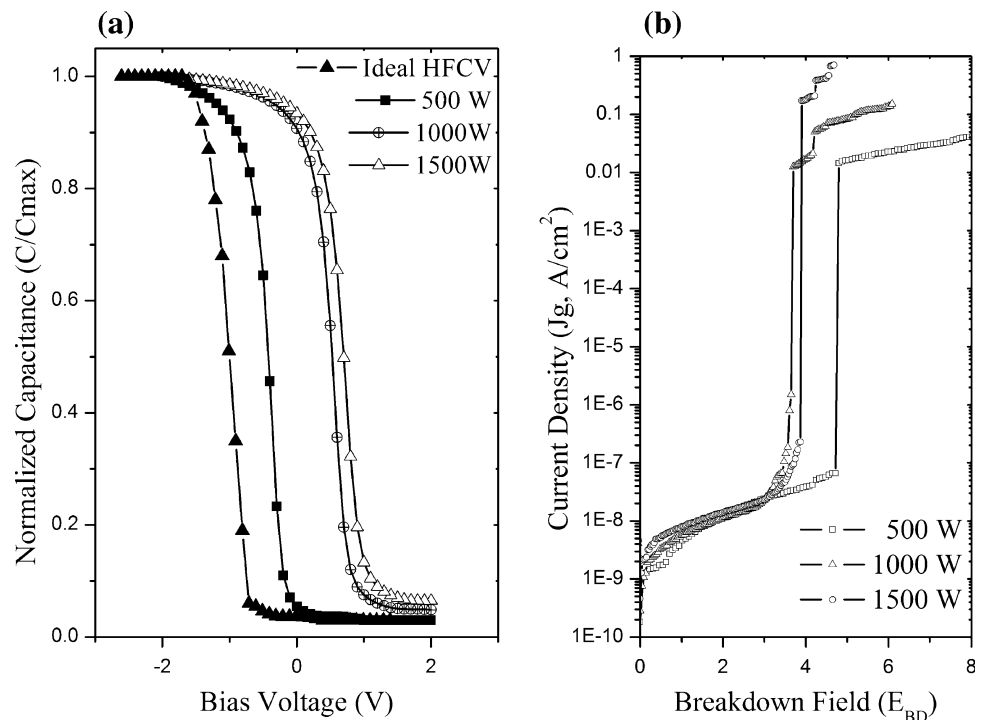
The impact of long duration anneals (60 s) at high temperatures (700/800/900°C) on the leakage characteristics of  $\text{Al}_2\text{O}_3$  have been examined. Figure 4 shows some interesting comparison of J–V characteristics obtained from the films before and after annealing.

In the above figure, a distinct trend in the leakage current was observed. The annealed films exhibited higher leakage current density than the unannealed sample, and the leakage current increases with increasing annealing temperature. This is believed to be due to two reasons: first,

**Fig. 1** **a** Variation in thickness and refractive index with power, before and after annealing. **b** Refractive index versus dielectric constant



**Fig. 2** **a** Normalized C–V plot, **b** J–E characteristics

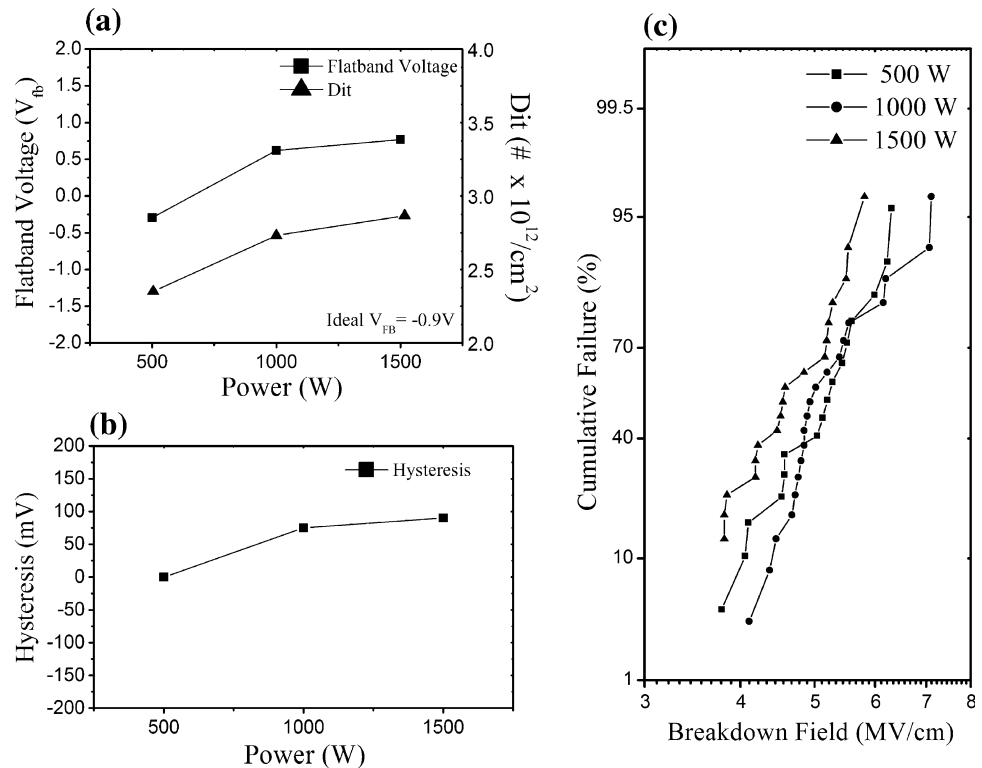


annealing render the films with a higher degree of crystallinity than the as-deposited films (as noticed by the RI and  $k$  values before and after annealing), the extent of which increases with the increasing time and temperature. Also, even though  $\text{Al}_2\text{O}_3$  has a bulk crystallization temperature of  $\sim 1,050^\circ\text{C}$  (Jakschik et al. 2003), lower film thickness and extended period of annealing cause the films

to crystallize at comparatively lower temperatures. Literature survey also provides a strong support to this argument (Jakschik et al. 2003).

The second and the significant reason, is the diffusion of oxygen into the film. It has been understood that oxygen from the gaseous phase diffuses into the film during annealing, and gets incorporated in near-surface and bulk

**Fig. 3** Plasma power versus **a** Flatband voltage and Dit, **b** hysteresis, **c** breakdown field versus cumulative failure



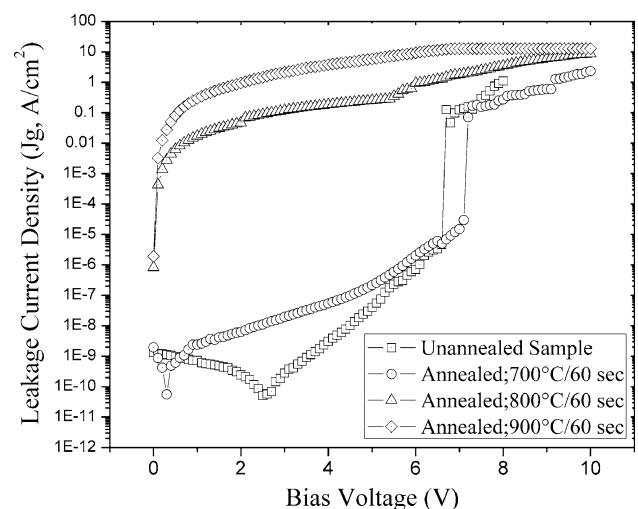
regions, to amounts and ranges which increases with increasing annealing time and temperature (Houssa 2004). This oxygen arrives at the interface where it reacts with the bulk silicon and forms silicon oxide. The oxidized silicon occupies a larger volume and, in turn, generates interstitial Si in mobile state (Monagham 2007). Hence, oxidation of silicon not only transforms oxygen from mobile state to fixed state, but also renders some silicon from fixed to mobile species. This mobile silicon spreads towards bulk Si and  $\text{Al}_2\text{O}_3$  regions. Moreover, when in the  $\text{Al}_2\text{O}_3$  region, mobile Si atoms may displace Al, since silicon oxide formation is thermodynamically favored over that of aluminum oxide [standard enthalpy of formation of (a)  $\text{Al}_2\text{O}_3$ :  $-1670\text{ kJ/mol}$  (b)  $\text{SiO}_2$ :  $-860\text{ kJ/mol}$ ] (Skinner 1964). This reaction implies fixing mobile Si in the original  $\text{Al}_2\text{O}_3$  region and transforming fixed Al and O from the  $\text{Al}_2\text{O}_3$  network to mobile states. Also, mobile Si that migrated to the  $\text{Al}_2\text{O}_3$ /gate electrode interface may alter the Fermi level and the electrical conductivity (Krug et al. 2000).

Further, to investigate the behavior under stress of the mobile charge carriers thus generated, stress C–V analysis was performed on the annealed samples, and compared with the unannealed ones.

As can be seen from Fig. 5a, the unannealed sample shows a very slight shift in the C–V curve towards the more negative value with increasing stress time. This indicates the generation of very limited positive charge carriers during the electrical stress. These positive charges

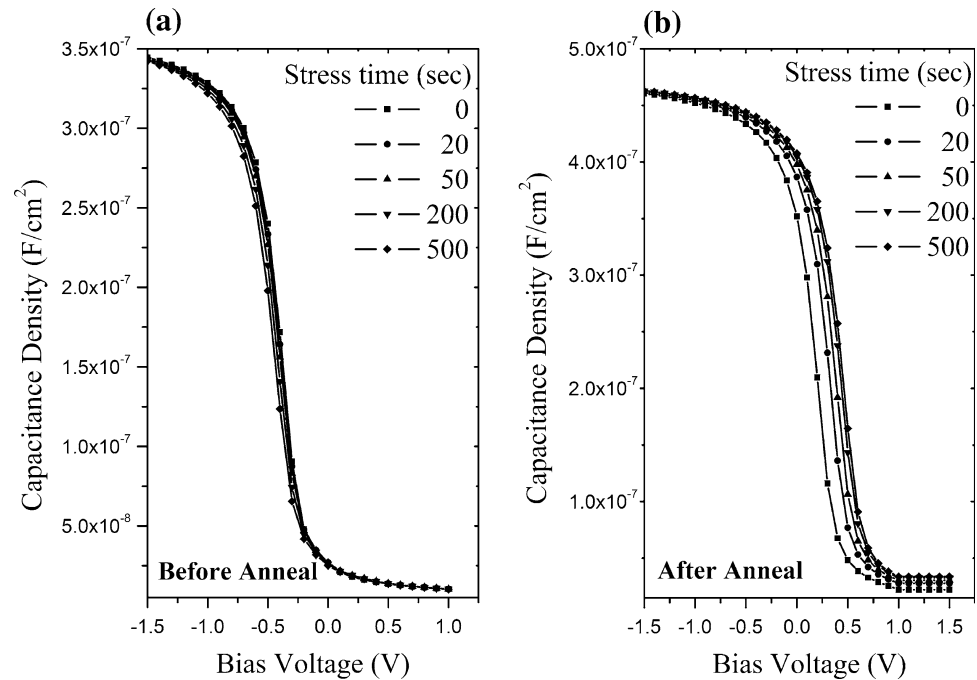
may have resulted from the trapping of positive species at pre-existing defects.

Figure 5b shows the shift in C–V curves of the annealed sample with respect to increasing stress time. Noteworthy fact here is the substantial shift towards the right or to the more positive values with increasing stress time, which implies that considerable amount of mobile charges are generated during the stress period. This fact further



**Fig. 4** Behavior of J–V characteristics of unannealed sample and annealed samples with increasing annealing temperature

**Fig. 5** Stress C–V behavior  
**a** before anneal **b** after anneal



corroborates the interaction between  $\text{Al}_2\text{O}_3$  and Si generating charge carriers in the dielectric, and the situation only exacerbates under the applied stress conditions.

## Conclusions

From the experiments reported here, it can be concluded that for a PVD process a low power deposition is favorable in terms of interface density, flatband voltage, hysteresis and cumulative failure. Also, although annealing has commonly been used to improve the as-deposited film's material and electrical characteristics, it has been demonstrated that longer duration anneals at higher temperatures have detrimental effect on the film's characteristics because of the generation of charge carriers through a complex process.

**Acknowledgments** Part of the reported work (fabrication/characterization) was carried out at the Center of Excellence in Nanoelectronics, Indian Institute of Technology, Bombay under Indian Nanoelectronics Users' Program which has been sponsored by Department of Information Technology, Ministry of Communications and Information Technology (Government of India). The authors would like to acknowledge Dr. Anil Kottantharayil and his graduate students at the Indian Institute of Technology, Bombay for their technical inputs.

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